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EXAMINER	
PARKER, JOHN M	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/786,070	ITO, TOYOJI	
	Examiner	Art Unit	
	John M. Parker	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20-30* is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☒ Claim(s) *16-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/26/04, 1/19/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants admitted prior art (AAPA) in view of Kanegae et al. (US Pat. Pub. 2002/0061654).

Regarding claim 1 AAPA teaches a method for fabricating a semiconductor device, the method comprising the steps of:

forming a conductive film on a substrate [fig. 16a, 12];

forming an insulating film such that the conductive film is covered with the insulating film [fig. 16b, 14];

AAPA fails to disclose the further steps of masking and etching an opening in the insulating layer. However, Kanegae teaches forming, in the insulating film, a hole having a bottom portion not reaching the conductive film [fig. 23b, 16] by using a mask layer having a first opening pattern [fig. 23b, 15a]; and

forming, in the insulating film, an opening for exposing the conductive film by using a mask layer having a second opening pattern having an opening diameter larger than an opening diameter of the first opening pattern [fig. 23c shows a wider mask

opening as well as the opening extending to the substrate below, pg. 1, paragraph [0017] explains the widened mask pattern],

an obtuse angle being formed between a wall surface of the opening and a bottom surface of the opening [fig. 23d, the obtuse angle is arranged between the top and bottom of the opening].

It would have been obvious to one of ordinary skill in the art to combine the teachings of AAPA and Kanegae to enable the method step of etching an opening in an oxide layer to be performed according to the teachings of Kanegae. One of ordinary skill in the art would have been motivated to look to analogous art teaching alternative suitable or useful methods of performing the disclosed method step of forming an opening in an oxide layer, art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Regarding claim 2, AAPA in view of Kanegae discloses the method of claim 1, further comprising the step of:

forming, at least in the opening, a capacitor element composed of a lower electrode [AAPA, fig. 17c, 16], a capacitor insulating film [AAPA, fig. 17c, 17], and an upper electrode [AAPA, fig. 17c, 18].

Regarding claim 3, AAPA in view of Kanegae teaches the method of claim 2, wherein the step of forming the capacitor element includes the steps of:

forming the lower electrode such that the wall surface of the opening and the bottom surface of the opening are covered with the lower electrode [AAPA, fig. 17c, 16];

forming the capacitor insulating film on the lower electrode [AAPA, fig. 17c, 17]; and

forming the upper electrode on the capacitor insulating film [AAPA, fig. 17c, 18].

Regarding claim 4, AAPA in view of Kanegae discloses the method of claim 3, wherein each of the lower electrode and the upper electrode contains a platinum group element as a main component [AAPA, pg. 2, lines 12-24].

Regarding claim 5, AAPA in view of Kanegae teaches the method of claim 3, wherein the capacitor insulating film is composed of a ferroelectric film or a high dielectric film [AAPA, pg. 2, lines 12-24].

Regarding claim 6, AAPA in view of Kanegae fails to specifically disclose the capacitor insulating film is composed of $SrBi_2(Ta_xNb_{1-x})_2O_9$, $Pb(Zr_xTi_{1-x})O_3$, $(Ba_xSr_{1-x})TiO_3$, $(Bi_xLa_{1-x})_4Ti_3O_{12}$ (where X satisfies a relationship represented by $0 \leq x \leq 1$), or Ta_2O_5, however AAPA in view of Kanegae does teach a bismuth layer-structured Perovskite-type oxide, the components of which are strontium, bismuth, tantalum, and niobium [AAPA, pg. 2, lines 17 and 18]. Mere selection of specific materials that are well known in the art are rendered obvious upon the basis of suitability for intended use. See *In re Leshin*, 125 USPQ 416 (CCPA 1960).

Regarding claim 7, AAPA in view of Kanegae teaches the method of claim 3, wherein the conductive film is composed of iridium, platinum, gold, ruthenium, rhodium, palladium, or a metal oxide thereof or alternatively composed of titanium, titanium-aluminum, tantalum, tantalum-aluminum, a nitride thereof, or a multilayer film composed thereof [AAPA, pg. 1, lines 21 and 22].

Regarding claim 8, AAPA in view of Kanegae discloses the method of claim 3, wherein the conductive film contains an oxygen barrier film [AAPA, fig 16a, 13].

Regarding claim 9, AAPA in view of Kanegae teaches the method of claim 3, wherein the insulating film is an oxide film containing silicon [AAPA, pg. 2, line 3].

Regarding claim 10, AAPA in view of Kanegae teaches the method of claim 3, wherein the insulating film has a planarized principal surface [AAPA, pg. 2, lines 4 and 5].

Regarding claim 11, AAPA in view of Kanegae fails to teach the method of claim 3, wherein the mask layer is a photoresist. However, the examiner takes official notice that it is notoriously well known in the art to a use photoresist material as a masking layer in the formation of openings.

Regarding claim 12, AAPA in view of Kanegae discloses a method for fabricating a semiconductor device, the method comprising the steps of:

Forming a conductive film on a specified region of a substrate [AAPA, fig. 16a, 12];

Forming an insulating film on the substrate such that the conductive film is covered with the insulating film [AAPA, fig. 16a, 14];

Forming, on the insulating film, a mask layer [Kanegae, fig. 23a, 15] having a first opening pattern above the conductive film [Kanegae, fig. 23a, 15a];

Performing first etching with respect to the insulating film by using the mask layer having the first opening pattern to form, in the insulating film, a depressed portion having a bottom portion not reaching the conductive film[Kanegae, fig. 23b, 16];

Forming a mask layer having a second opening pattern having an opening diameter larger than an opening diameter of the first opening pattern by enlarging the opening diameter of the first opening pattern [Kanegae, fig. 23c shows a wider mask opening as well as the opening extending to the substrate below, pg. 1, paragraph [0017] explains the widened mask pattern]; and

Performing second etching with respect to the insulating film by using the mask layer having the second opening pattern to form, in the insulating film, an opening for exposing the conductive film such that the opening has a diameter larger than a diameter of the depressed portion and a wall surface having a tapered configuration [fig. 23c shows a tapered opening, which when created opens the insulating layer to the layer below].

Regarding claim 13, AAPA in view of Kanegae teaches the method of claim 12, further comprising the step of:

forming, at least in the opening, a capacitor element composed of a lower electrode [AAPA, fig. 17c, 16], a capacitor insulating film [AAPA, fig. 17c, 17], and an upper electrode [AAPA, fig. 17c, 18].

Regarding claim 14, AAPA in view of Kanegae discloses the method of claim 13, wherein the step of forming the capacitor element includes the steps of:

forming the lower electrode such that the wall surface of the opening and the bottom surface of the opening are covered with the lower electrode [AAPA, fig. 17c, 16];

forming the capacitor insulating film on the lower electrode [AAPA, fig. 17c, 17]; and

forming the upper electrode on the capacitor insulating film [AAPA, fig. 17c, 18].

Regarding claim 15, AAPA in view of Kanegae fails to specifically disclose the first opening pattern is formed into a tapered configuration. However, the examiner takes official notice it is notoriously well known in the art that depending on the style of opening being created the opening pattern can be configured (angle, width, etc) to suit the need.

Allowable Subject Matter

Claims 20-30 are allowed.

Claims 16-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 16,18 and 19, the prior art does not teach or suggest a third etching stop following the removal of the mask layer for the purpose of smoothing the tapered configuration of the opening.

Regarding claim 17, the prior art does not teach or suggest a third opening pattern with a larger diameter than the second opening pattern and performing a third etching to smooth the tapered configuration of the opening

Regarding claims 20-26, the prior art does not disclose an etch stop layer nor a third etching step for removing the etch stop layer in the opening , exposing the conductive film and smoothing the tapered configuration.

Regarding claims 27-30, the prior art does not teach a second etch without a mask layer which results in an opening having a larger diameter than the diameter of the depressed portion and a wall surface having a tapered configuration

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additional cited art teaches similar methods to those instantly claimed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M. Parker whose telephone number is 571-272-8794. The examiner can normally be reached on Monday - Friday 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John M. Parker

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